REMARKS

Claims 1-16 and 21-22 are pending. By this amendment, claims 1 and 16 are amended and claim 23 is canceled. Applicants respectfully request reconsideration and timely withdrawal of the pending objections and rejections for the reasons discussed below.

Pursuant to MPEP §714.13, Applicants contend that entry of the present amendment is appropriate because the proposed amended claims avoid the rejections set forth in the last Office Action, resulting in the application being placed in condition for allowance, or, alternatively, the revised claims place the application in better condition for purposes of appeal. Furthermore, the revised claims do not present any new issues that would require any further consideration and/or search by the Examiner, and the amendment does not present any additional claims without cancelling a like number of pending claims. The features of claim 23 are incorporated into claims 1 and 16. Accordingly, entry of the present amendment is respectfully requested.

35 U.S.C. §102(e) Rejection

Claims 1 and 23 are rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Patent Application No.: 2004/0097030 to Sayama, *et al.* This rejection is respectfully traversed.

Applicants submit that the rejections of claims 1 and 23 are rendered moot in view of the submitted Declaration under 37 C.F.R. §1.131, by the named inventors. Under § 1.131, a rejection under 35 U.S.C. §102(e) based on a U.S. patent or publication may, upon a proper showing, be overcome by removing the patent or publication as a reference against the claims. Applicants submit that the §1.131 Declaration submitted herewith is sufficient to remove the Sayama publication as a reference and thus is sufficient to overcome the above-noted rejections.

Applicants submit that the §1.131 Declaration is formally and substantively sufficient to establish that the Inventors had completed the invention defined in at least claims 1 and 23 in a WTO country before the effective date of the Sayama reference, i.e., July 17, 2003. The statements in the Declaration show that the formal requirements of §1.131 are satisfied, namely:

(1) the rejections to be overcome are under §102(e), and

(2) all the acts for completing the invention of claims 1 and 23 were performed in the United States.

It is respectfully submitted that the statements in the Declaration are also sufficient to satisfy the substantive requirements of 37 C.F.R. §1.131. The Declaration sets forth specific facts, of sufficient character and weight, to establish a **date of conception** before July 17, 2003, the effective date of the Sayama reference, and to show that the Inventors and their attorneys exercised **due diligence** from a time before the effective date of the Sayama reference to a constructive reduction to practice, i.e., to the filing date of the application in the United States

As stated in the Declaration, the Inventors conceived a method for manufacturing an integrated circuit comprising a plurality of semiconductor devices including an n-type transistor and a p-type transistor on a semiconductor wafer before the effective date of the Sayama reference. An IBM Invention Disclosure is submitted with the Declaration as supporting evidence of this prior date of conception. It is respectfully submitted that the Invention Disclosure shows that the Inventors had a definite and permanent idea of the complete and

operative invention of claims 1 and 23, as presently pending, prior to July 23, 2003, the effective date of the Sayama reference.

In particular, the Invention Disclosure and other documents show the features of claims 1 and 23. Also, Applicants note that the original Invention Disclosure shows a date antedating the July 17, 2003 effective date of the Sayama reference. This and all other pertinent dates have been removed from the photocopies of the Invention Disclosure submitted with the Declaration to prevent any potential prejudice to Applicants. Applicants further submit that the Declaration filed herewith shows, unequivocally, that the Inventors had in their possession a definite and permanent idea of the complete and operative invention of claims 1 and 23 before July 17, 2003 in a manner sufficient to satisfy the requirements of conception, as set forth in M.P.E.P. §§ 715.07 and 2138.04, and thus constitute *prima facie* evidence of Applicants' date of conception of the invention in this country before the effective date of the Smith reference.

Applicants further submit that the Declaration shows the Inventors and their attorneys exercised due diligence from a time before the July 17, 2003 effective date of the Sayama reference to a constructive reduction to practice, realized by the filing of the above-identified patent application on September 23, 2003 in the U.S. Patent Office. For example, the Invention Disclosure was forwarded to outside counsel in a timely manner. Discussions between the Inventors and counsel took place until a final application was forwarded to the Inventors for execution, and subsequent filing on September 23, 2003.

Counsel acted in an expeditious manner to prepare the application for filing. Under M.P.E.P. §2138.06, only ***reasonable*** diligence is required in this regard. More specifically, §2138.06 states that a patent attorney will be held to have exercised reasonable diligence if the

attorney worked reasonably hard on the application during the critical period, taking into consideration any backlog of unrelated cases the attorney may have had and his completion of those cases along with the present application in chronological order. Applicants respectfully submit that the Declaration shows that counsel acted sufficiently expeditiously to satisfy the requirements of due diligence.

Applicants submit that the Declaration submitted herewith is sufficient to show that due diligence was exercised as required under 37 C.F.R. § 1.131. The Inventors remained in regular contact with counsel to answer questions, provide technical explanation, and supply materials necessary for allowing the application to be filed in an expeditious manner.

35 U.S.C. § 103 Rejection

Claims 1, 3-5, 12, 14-16 and 22 are rejected under 35 U.S.C. § 103(a) as being unpatentable over U. S. Patent No. 6,288,694 issued to Doyle, *et al.* ("Doyle"). Claim 2 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Doyle *et. al.,* in view of U. S. Patent No. 4,517,731 issued to Khan, *et al.* ("Khan"). Claims 1, 3-16, and 21-22 are rejected under 35 U.S.C. Section 103(a) as being unpatentable over U.S. Patent No.: 6,204,103 to Bai, *et al.* in view of Doyle. These rejections are respectfully traversed.

Claims 1 and 16

Claims 1 and 16 recite oxidizing a portion of a gate polysilicon of the n-type transistor, such that tensile mechanical stresses are formed within a channel of the n-type transistor. Claim 16 further recites that the oxidizing is performed without creating additional tensile stresses in a

channel of the p-type field effect transistor. The oxidizing step results in formation of a bird's beak in an edge of the gate polysilicon.

Doyle, at Figures 5-7, discloses creating voids *in a substrate* before either an n-type or a p-type transistor is formed. Additionally, at Figures 8-10, Doyle discloses creating voids within the *source and drain regions* of a substrate after an n-type or a p-type transistor is formed. Also, Doyle discloses, in Figures 11–13, creating voids *in a polysilicon gate* after an n-type or a p-type transistor is formed. In Figure 17, Doyle discloses a single void 142 formed in a channel region. In Figure 18, Doyle discloses multiple voids 152 formed at the outer edges of a channel region. However, Doyle, does not disclose the formation of a bird's beak in an edge of the gate polysilicon. Consequently, Doyle fails to disclose or suggest the recited elements of claims 1 and 16.

As to the rejection over the combination of Bai in view of Doyle, Applicants submit that this combination does not teach or suggest the formation of a bird's beak in an edge of the gate polysilicon. For these reasons, claims 1 and 16 are allowable over Bai and Doyle, whether alone or in combination. Accordingly, allowance of claims 1 and 16 is respectfully requested.

Claims 2-15, 21 and 22

Claims 2-15, 21 and 22 are allowable over the cited reference based on their dependencies from an allowable base claim. Additionally, claims 14 and 15 are further allowable based on their additional features.

Claims 14 and 15 recite that the step of oxidizing comprises oxidizing the gate polysilicon of the n-type field effect transistor to create a stress of about 700MPa in a channel of the n-type field effect transistor or about 500Pa to about 1000Pa. Despite the previously submitted arguments, the Examiner maintains that the claimed tensile stress ranges lack criticality because Applicants do not teach that the tensile stress ranges solve any stated problem or are for any particular purpose. Applicants again respectfully traverse this submission, and direct the Examiner's attention to Figures 4 and 5, as well as to page 2 of the specification, where it is stated that tensile stresses in conventional n-type devices are relatively moderate (i.e., for example, about 200 MPa to about 300 MPa). Comparing the results of Figures 4 and 5 to these conventional results, it is seen that embodiments of the present invention offer improved tensile stress ranges, which are in embodiments are critical to their operation.

Additionally, Applicants further direct the Examiner's attention to page 10 of the specification, where it is noted:

> the oxidation of the gate of the NFETs creates large tensile stresses in the channel region of the NFETs ... Further, these tensile stresses increase electron mobility along the channel, and improve the performance of the NFETs.

At page 13, it is noted that the desired stresses are tensile and add values of the order of 200MPa and above. For these reasons, and because the cited references disclose a tensile stress of about 100 MPa, the tensile stress ranges recited in claims 14 and 15 are allowable. Consequently, allowance of claims 14 and 15 is respectfully requested.

CONCLUSION

In view of the foregoing amendments and remarks, Applicants submit that all of the claims are patentably distinct from the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue. The Examiner is invited to contact the undersigned at the telephone number listed below, if needed. Applicants hereby make a written conditional petition for extension of time, if required. Please charge any deficiencies in fees and credit any overpayment of fees to **IBM Deposit Account No. 09-0458**.

Respectfully submitted,

Andrew M. Calderon
Reg. No. 38,093

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Suite 1800
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Disclosure FIS-2003-0053

Prepared for and/or by an IBM Attorney - IBM Confidential

Created By DURESETI CHIDAMBARRAO
Last Modified By Judy Paolillo

Required fields are marked with the asterisk (*) and must be filled in to complete the form .

***Title of disclosure (in English)**
Mechanically Improved Damascene Gate nFETs

Summary

Status		Awaiting Search
Final Deadline		
Final Deadline Reason		
*Processing Location		Fishkill
*Functional Area	select	(ISA) Issac
Attorney/Patent Professional		Joseph P Abate/Fishkill/IBM
IDT Team	select	Oleg Gluschenkov/Fishkill/IBM William Devine/Fishkill/IBM DOMINIC SCHEPIS/Fishkill/IBM David Hanson/Fishkill/IBM Thomas Dyer/Fishkill/IBM Noah Zamdmer/Fishkill/IBM DURESETI CHIDAMBARRAO/Fishkill/IBM Werner Rausch/Fishkill/IBM Samuel Fung/Fishkill/IBM
Submitted Date		
*Owning Division	select	MD
Incentive Program		
Lab		
*Technology Code		101N2
PVT Score		38

Inventors with a Blue Pages entry

Inventors: Omer Dokumaci/Fishkill/IBM, DURESETI CHIDAMBARRAO/Fishkill/IBM, Oleg Gluschenkov/Fishkill/IBM

Inventor Name	Inventor Serial	Div/Dept	Inventor Phone	Manager Name
> Dokumaci, Omer H.	795369	29/62GD	532-4893	Oldiges, Philip (Phil)
Chidambarrao, Dureseti (Chidu)	254149	29/4S2A	532-2336	Li, Yujun
Gluschenkov, Oleg G.	2A1177	29/38YA	532-9788	Crabbe, Emmanuel

> denotes primary contact

Inventors without a Blue Pages entry

IDT Selection
***Main Idea**

1. Background: What is the problem solved by your invention? Describe known solutions to this problem (if any). What are the drawbacks of such known solutions, or why is an additional solution required? Cite any relevant technical documents or references.

Stresses are known to enhance device characteristics. We have submitted many disclosures (FIS8-2001-0377, FIS8-2001-0430, FIS8-2001-0453, for example) where we control stress through STI and spacers. We use different material combinations to apply the tensile stress for the nFET and the compressive stress for the pFET that are needed along the channel direction. In all these disclosures the stresses in the channel are relatively moderate (typically 200-300MPa) which while providing a 10% benefit are still limited.

Oxidation of silicon, when confined, is known to create very large stresses in silicon. We use oxidation of the gate polysilicon to control the stresses in CMOS nFET devices such that their performances are enhanced without degrading the performance of the PFET devices.

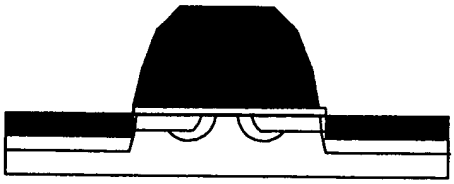
2. Summary of Invention: Briefly describe the core idea of your invention (saving the details for questions #3 below). Describe the advantage(s) of using your invention instead of the known solutions described above.
After a planarizing oxide is formed, the NFET poly is oxidized to create a large tensile stress in the channel (~700 MPa). This stress improves the mobility of electrons. PFET is masked to prevent any degradation of hole mobility from this process.

Oxidation of polysilicon creates larger stresses in the channel than STI and spacer approaches. This lets us improve NFET mobility further.

3. Description: Describe how your invention works, and how it could be implemented, using text, diagrams and flow charts as appropriate.

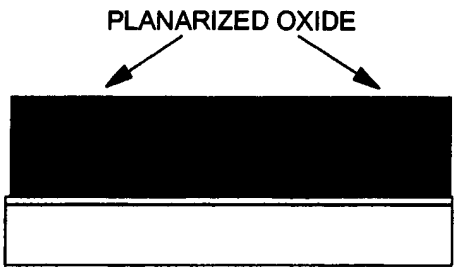
PROCESS FLOW
---

1) START AFTER THE SILICIDATION STEP

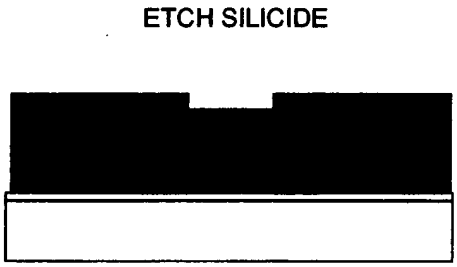


The strating structure can alternatively have a nitride cap on top of the gate. In that case, there will not be any silicide on top of the gate. In step #3, the nitride cap can be etched off instead of the silicide.

2) OXIDE PLANARIZATION

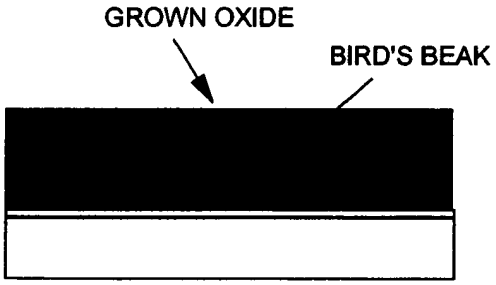


3) ETCH SILICIDE



After this step, a hard mask like nitride is deposited. NFETs are exposed and PFETs are masked. Nitride is etched off from the NFET region. So, steps 4&5 does not affect the PFETs.

4) OXIDATION



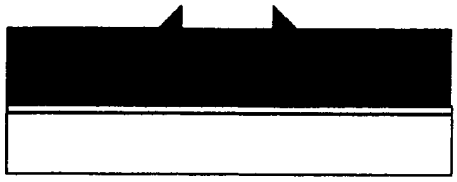
Oxidation of the gate creates a big tensile stress in the channel region (Figure 1). This tensile stress increases electron mobility.

This step requires low temperature oxidation such as high pressure oxidation or plasma oxidation. Low thermal budget is needed so that the device characteristics will not be degraded by deactivation or diffusion.

Since PFETs are masked by the nitride, the PFET gate poly will not be oxidized. After this step, nitride covering the PFETs is etched off.

5) ETCH OXIDE

ETCH OXIDE



As shown in Fig.2 , the stress in the channel remains even after etching off the top oxide. The stress is caused by the vertical bird's beak that forms in the poly.

6) SILICIDATION

GROW SILICIDE

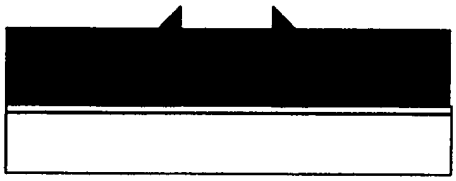


Figure 1. Stresses in the silicon structure after gate polysilicon oxidation. (Magenta - 700MPa; Solid - Compression; Dashed - Tension)

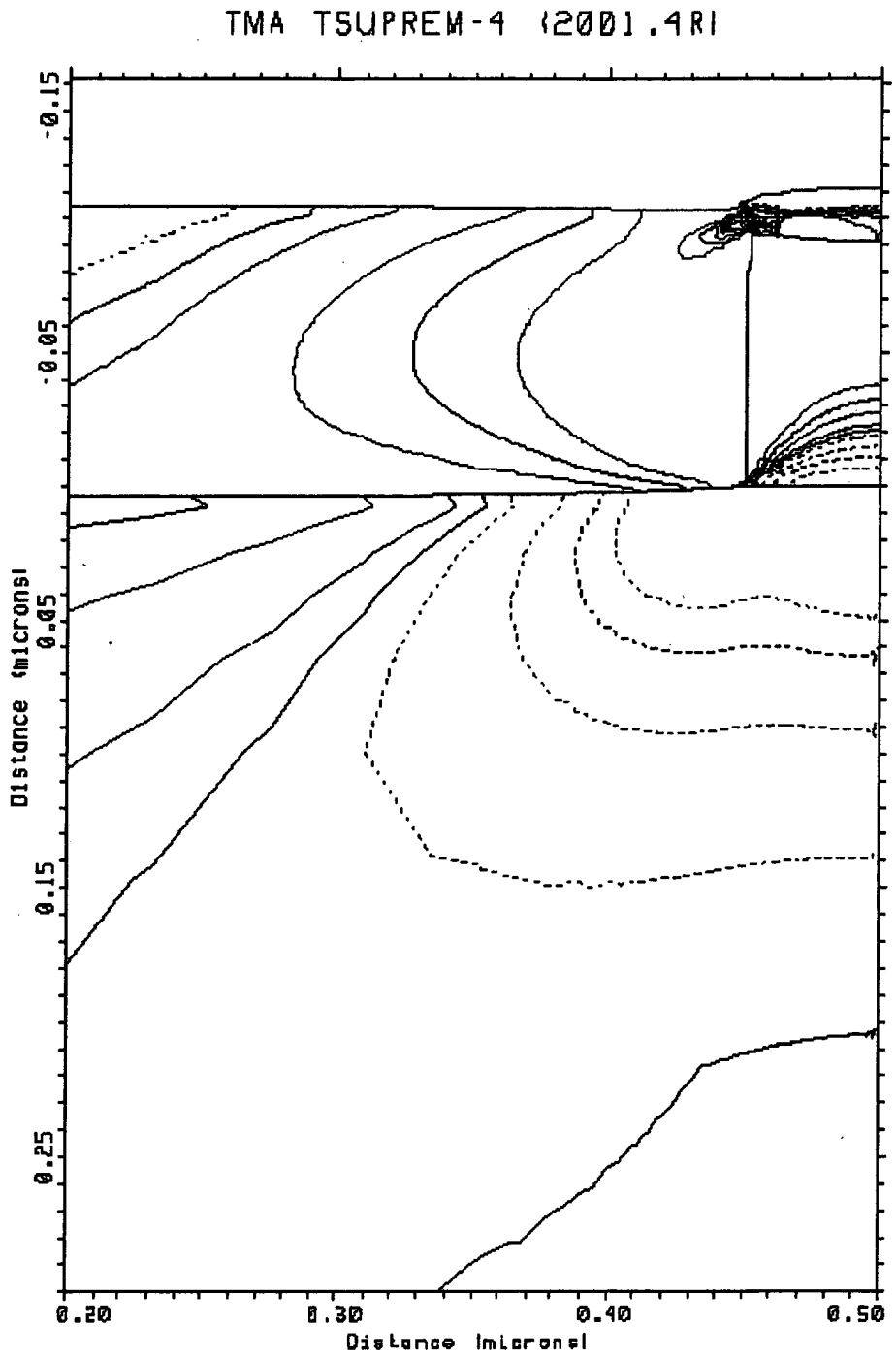
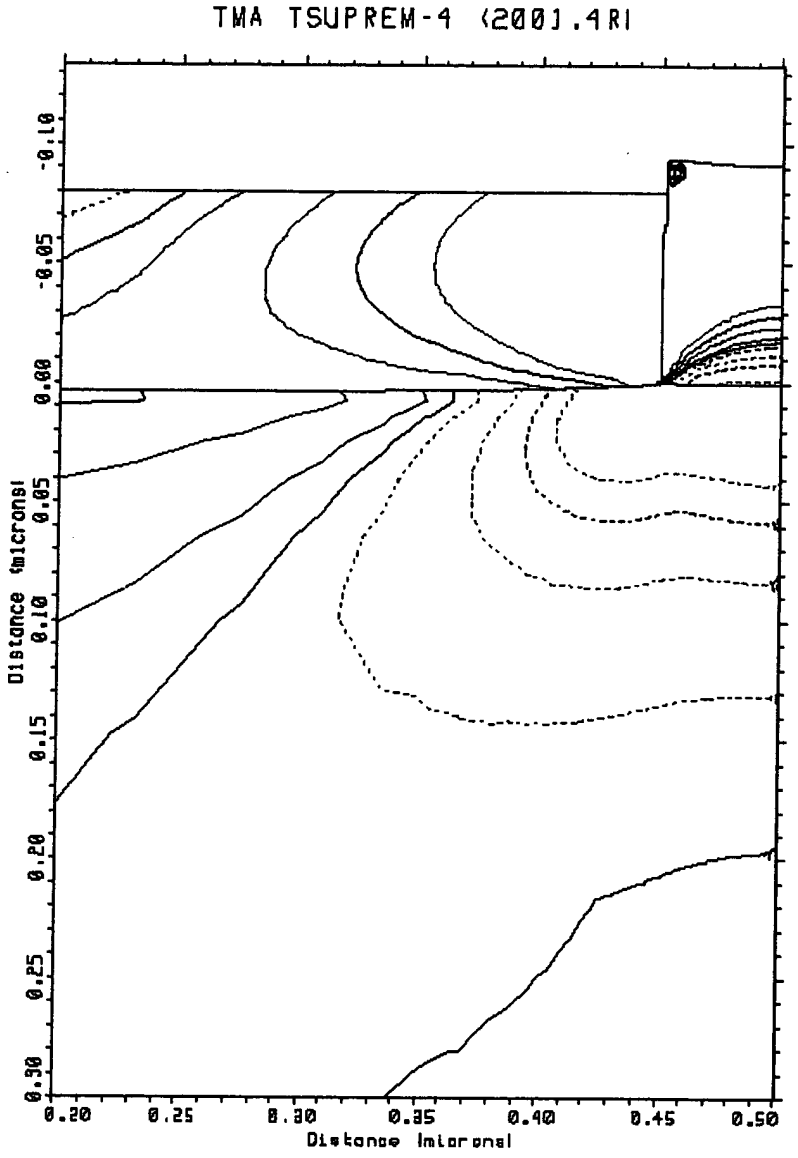


Figure 2. Stresses remain in silicon structure after gate polysilicon oxidation because of vertical bird's beak that forms. (Magenta -

700MPa; Solid - Compression; Dashed - Tension)



***Patent Value Tool**

* **1.** Select the single most appropriate technology category for your invention from the following technologies list.
(101N2) PPM 100 Solid State Technologies-101N2 FET; CMOS devices . . .
Comments
Are there any additional significant markets where the invention is likely to have impact?
○ Yes ● No

*2. Have you implemented the invention (e.g., made a prototype) or otherwise shown that it is workable?
○ Yes ● No

*3. Has the subject matter of the invention or a product incorporating the invention been offered for sale, or is it likely to be offered for sale, as part of an IBM product or service?
● No known product plans within 2 years
○ Maybe; GA 1-2 years away
○ Yes; GA within 3-12 months
○ Yes; GA within 3 months
○ Yes; product has been announced

*4. Has the invention been commercially used (internally or externally) by IBM or another entity (e.g., included in or used to make products, or prototypes provided to a customer)?
○ Yes ● No

*5. In what type of product might a competitor include the invention?
Advanced Logic Technologies, like 10S2, 11S, 10SF and further

What competitor(s) (indicate home country of such competitors if not United States)?
All semiconductor companies

*6. How easily can the use of the invention by a third party be detected?
○ Undiscoverable; third party must admit use for IBM to know
○ Difficult; e.g.; with reverse engineering or examination of available code
● With work; e.g.; using test cases; but not reverse engineering
○ Easily; by running & viewing product operation
○ Trivally; without purchase of product; e.g.; by reading product literature

Please propose how a test would be performed and what test methods may be required:
SEM, TEM

*7. Is the invention applicable to a standard?
○ Yes ● No

*8. Have you, or any of the other inventors, submitted this invention disclosure or a similar invention disclosure previously?
○ Yes ● No

*9. Please list the invention disclosures (previously submitted or about to be submitted), products, patents, or publications that you and the other inventors feel are the most relevant to your invention (e.g., pertaining to the problem you are solving, including other solutions to the problem), be they from you or anyone else, or if not applicable, enter "None":
None

* 10. Was the invention made in the course of any activity that involved any other party, be it
- The government
- A customer (such as an RFQ)
- A development partner
- An alliance
- Any contract activity
- As part of a standards setting activity
- Other persons not employed by IBM

○ Yes ● No

*11. Have you ever disclosed your invention to anyone outside IBM, or do you plan to do so in the

future?
○ Yes ● No

12. If the invention relates to a product or service that is outside the scope of your business unit, please recommend IBM business unit(s), IBM location(s) or individual(s) within IBM that you think would provide a competent evaluation of your invention:

***PVT II**

All of the questions below are required and must be answered in order to calculate a PVT Score
A.Threshold Questions

***1. Operability** - Is there an identifiable operable embodiment of the invention (i.e., an embodiment that has been demonstrated or that would be reasonably expected to provide the benefits of the invention)?
● Yes ○ No

Reasons for above answer:

***2. Novelty**- Are one or more concept(s) of the invention novel over what is already known in the literature, existing commercial products, patents, and earlier IBM invention disclosures?
● Yes ○ No
Reasons for above answer:

B.Valuation Questions

***1.** Adequacy of Description:
○ Inadequate; invention unclear from description
○ Incomplete; essential features missing
○ Further clarification or implementation detail needed
● Clear and complete as is
State reason for answer:

***2.** Technical contribution of invention:
○ None
○ Minor addition to known technology
● Significant addition to known technology
○ Major advance in technology
Reasons for above answer:

***3.** Describe the problem solved/benefit provided and the implementation cost of the invention compared to existing or reasonably expected alternatives:
○ Minor problem/incremental benefit - significant implementation cost
● Significant problem; substantial benefit - significant implementation cost
○ Minor problem/incremental benefit - minor implementation cost
○ Significant problem/substantial benefit - minor implementation cost

***4.** Are any alternatives to the invention available to those wishing to avoid its use?
○ Suitable alternatives available
● Alternatives have drawbacks
○ No feasible alternatives
Reasons for above answer:

*5. Describe the likelihood of use of the invention (answer each):

IBM's customers?	○ Unlikely	● Possible	○ Probable	○ Definite
IBM's suppliers/vendors?	● Unlikely	○ Possible	○ Probable	○ Definite
IBM's competitors?	○ Unlikely	● Possible	○ Probable	○ Definite
IBM?	○ Unlikely	● Possible	○ Probable	○ Definite

Reasons for above answer:

*6. What % of third party products in the technical field will likely contain the invention?

○ < 25%
○ 25-50%
● 50-75%
○ > 75%

Reasons for above answer:

*7. How long is the invention likely to be used in products by IBM or others?

○ < 5 years
○ 5-10 years
● 10-15 years
○ > 15 years

Reasons for above answer:

*8. How easily can use of the invention by a third party be detected?

○ Undiscoverable; third party must admit use for IBM to know
● Difficult; e.g.; with reverse engineering or examination of available code
○ With work; e.g.; using test cases; but not reverse engineering
○ Easily; by running & viewing product operation
○ Trivially; without purchase of product; e.g.; by reading product literature

Reasons for the above answer, including description of how use could be detected:

Evaluation

This evaluation was entered by **Judy Paolillo/Fishkill/IBM**

Team Evaluation
What is the team's evaluation of this disclosure? Search
Date rated :
Evaluation Comments

Final Evaluation History	Who made the final evaluation	Final evaluation date
Search	Judy Paolillo/Fishkill/IBM	

Search Information
Search Office Information
Post Disclosure Text & Drawings

Search Rec

JPA

IP&L Disclosure Evaluation: FIS8-2003-0053

Prepared for and/or by an IBM Attorney - IBM Confidential

Created By Oleg Gluschenkov
Last Modified By Oleg Gluschenkov

Required fields are marked with the asterisk (*) and must be filled in to complete the form.

Title of disclosure
Mechanically Improved Damascene Gate nFETs

Date evaluation due to IPL: 03/07/2003 | **Date evaluation submitted to IP&L: 05/01/2003**

A.Threshold Questions

1. Operability - Is there an identifiable operable embodiment of the invention (i.e., an embodiment that has been demonstrated or that would be reasonably expected to provide the benefits of the invention)?
● Yes ○ No

Reasons for above answer:

2. Novelty- Are one or more concept(s) of the invention novel over what is already known in the literature, existing commercial products, patents, and earlier IBM invention disclosures?
● Yes ○ No

Reasons for above answer:

B.Valuation Questions

1. Adequacy of Description:
○ Inadequate; invention unclear from description
○ Incomplete; essential features missing
○ Further clarification or implementation detail needed
● Clear and complete as is

State reason for answer:

2. Technical contribution of invention:
○ None
○ Minor addition to known technology
● Significant addition to known technology
○ Major advance in technology

Reasons for above answer:
Novel strained CMOS structure

3. Describe the problem solved/benefit provided and the implementation cost of the invention compared to existing or reasonably expected alternatives:
○ Minor problem/incremental benefit - significant implementation cost
● Significant problem; substantial benefit - significant implementation cost
○ Minor problem/incremental benefit - minor implementation cost
○ Significant problem/substantial benefit - minor implementation cost

4. Are any alternatives to the invention available to those wishing to avoid its use?

○ Suitable alternatives available

● Alternatives have drawbacks

○ No feasible alternatives

Reasons for above answer:

5. Describe the likelihood of use of the invention (answer each):

IBM's customers? ○ Unlikely ● Possible ○ Probable ○ Definite

IBM's suppliers/vendors? ● Unlikely ○ Possible ○ Probable ○ Definite

IBM's competitors? ○ Unlikely ● Possible ○ Probable ○ Definite

IBM? ○ Unlikely ● Possible ○ Probable ○ Definite

Reasons for above answer:

6. What % of third party products in the technical field will likely contain the invention?

○ < 25%

○ 25-50%

● 50-75%

○ > 75%

Reasons for above answer:

7. How long is the invention likely to be used in products by IBM or others?

○ < 5 years

○ 5-10 years

● 10-15 years

○ > 15 years

Reasons for above answer:

8. How easily can use of the invention by a third party be detected?

○ Undiscoverable; third party must admit use for IBM to know

● Difficult; e.g.; with reverse engineering or examination of available code

○ With work; e.g.; using test cases; but not reverse engineering

○ Easily; by running & viewing product operation

○ Trivially; without purchase of product; e.g.; by reading product literature

Reasons for the above answer, including description of how use could be detected:

Evaluator Recommended Decision : ○ Close ○ Publish ● Search

Close: A patent would probably have little licensing value or IBM's freedom of use is already assured or is not important.

Publish: A patent would probably have limited licensing value to IBM but freedom of use should be preserved.

Search: A patent on this subject could have significant licensing value. IPLaw should provide an option on patentability and portfolio value and a recommendation whether to file a patent application.

☐ Additional Search Info:This disclosure should be MERGED before searching and filing with disclosure (s)

Comments (Note : Limit your comments to technical/business issues)